CLAIM AMENDMENTS

1. (Original) An apparatus for responding to each edge of an input strobe signal by generating a corresponding edge in each of first and second strobe signals, wherein corresponding edges in the first and second strobe signals are separated by a target delay referenced by input data, the apparatus comprising:

a first multiplexer for receiving the input strobe signal and the first and second strobe signals, and for providing any one of the input, first and second strobe signals selected by first selection control data as a first multiplexer output signal;

a first circuit for generating the first and second strobe signals in response to the first multiplexer output signal such that each edge in the first multiplexer output signal subsequently produces a corresponding edge in the first and second strobe signals, with corresponding edges in the first and second strobe signals being separated in time by a programmable delay set by delay control data; and

a control circuit receiving the input data and the first multiplexer output signal for supplying the first selection control data to the first multiplexer and for supplying the delay control data to the first circuit.

2. (Original) The apparatus in accordance with claim 1 wherein the control circuit carries out a calibration process wherein it sets the delay control data so that the programmable delay between corresponding edges of the first and second strobe signals matches the target delay referenced by the input data.

3. (Original) The apparatus in accordance with claim 2 wherein following the calibration process, the control circuit sets the first selection control data so that the first multiplexer provides the input strobe signal as the first multiplexer output signal such that a next edge of the input strobe signal will result in corresponding edges in the first and second strobe signals separated in time by the target delay.

4. (Previously Presented) The apparatus in accordance with claim 2

wherein during the calibration process the control circuit generates count data indicating a difference between first and second quantities,

wherein the first quantity is a number of edges of a reference clock signal occurring during a first period determined by counting a predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer is providing the first strobe signal as the first multiplexer output signal, and

wherein the second quantity is a number of edges of a reference clock signal occurring during a second period determined by counting the predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer is providing the second strobe signal as the first multiplexer output signal.

5. (Original) The apparatus in accordance with claim 4, wherein during the calibration process the control circuit iteratively carries out a process of generating the count data, comparing the count data to the input data, and adjusting the delay control data to determine a value for the delay control data that sets the programmable delay equal to the target delay.

6. (Original) The apparatus in accordance with claim 4 wherein the control circuit decrements the count data in response to edges of the reference clock signal during the first period and increments the count data in response to edges of the reference clock signal during the second period.

7. (Original) The apparatus in accordance with claim 6, wherein during the calibration process the control circuit iteratively carries out a process generating the count data, compares the count data to the input data, and adjusting the delay control data to determine a value for the delay control data that sets the programmable delay equal to the target delay.

8. (Original) The apparatus in accordance with claim 7 wherein following the calibration process, the control circuit sets

the first selection control data so that the first multiplexer provides the input strobe signal as the first multiplexer output signal such that a next edge of the input strobe signal will result in corresponding edges in the first and second strobe signals separated in time by the target delay.

9. (Previously Presented) The apparatus in accordance with claim 6 wherein the control circuit comprises:

a first counter for counting edges of the first multiplexer output signal and for generating a gate signal indicating when the first and second periods are occurring;

a second counter for decrementing the count data in response to edges of the reference clock signal when the gate signal indicates the first period is occurring and for incrementing the count data in response to edges of the reference clock signal when the gate signal indicates the second period is occurring; and

means for incrementing or decrementing the delay control data depending on relative magnitudes of the count data and the delay data.

10. (Original) The apparatus in accordance with claim 1 wherein the first circuit comprises:

a tapped delay line having N taps for conveying the first multiplexer output signal to each of its N taps in succession, where N is greater than two;

a second multiplexer for providing the first multiplexer output signal conveyed to any one of the N taps selected by the delay control data as a second multiplexer output signal; and

first means for generating the first strobe signal in response to the second multiplexer output signal.

11. (Original) The apparatus in accordance with claim 10 wherein the first circuit further comprises:

second means for generating the second strobe signal in response to the first multiplexer output signal with a delay substantially matching a delay between an edge of the first multiplexer output signal arriving at any tap selected by the delay control data and a corresponding edge of the first strobe signal generated by the second means.

12. (Original) The apparatus in accordance with claim 10 wherein the first circuit further comprises:

a third multiplexer for providing the first multiplexer output signal conveyed to any one of the N taps selected by the delay control data as a third multiplexer output signal, wherein the delay control data independently controls the tap selection made by the second and third multiplexers; and

second means for generating the second strobe signal in response to the third multiplexer output signal.

13. (Original) The apparatus in accordance with claim 1 wherein the first circuit provides a first signal path for delaying the first multiplexer output signal with a first delay to produce the first strobe signal, the first delay being controlled by the delay control data,

wherein the first signal path includes a first number of gates,

wherein the delay control data controls a magnitude of the first number, and

wherein the first delay is a function of a sum of delays through the first number of gates.

14. (Original) The apparatus in accordance with claim 13 wherein a delay through each gate of the first number of gates is a function of the delay control data.

15. (Previously Presented) The apparatus in accordance with claim 13

wherein the first signal path comprises a first capacitor having an adjustable first capacitance,

wherein the delay control data controls the first capacitance, and

wherein the first delay is a function of the first capacitance.

16. (Previously Presented) The apparatus in accordance with claim 10

wherein the first circuit provides a second signal path for delaying the second multiplexer output signal with a second delay to produce the second strobe signal, the second delay being controlled by the delay control data,

wherein the second signal path includes a second number of gates,

wherein the delay control data controls a magnitude of the second number, and

wherein the second delay is a function of a sum of delays through the second number of gates.

17. (Original) The apparatus in accordance with claim 16 wherein a delay through each gate of the first number of gates is variable and a function of the delay control data, and

wherein a delay through each gate of the second number of gates is variable and a function of the delay control data.

18. (Original) The apparatus in accordance with claim 16 wherein the first signal path comprises a first variable capacitor,

wherein the delay control data controls a first capacitance of the first variable capacitor, and

wherein the first delay is a function of the first capacitance.

wherein the second signal path comprises a second variable capacitor,

wherein the delay control data controls a second capacitance of the second variable capacitor, and

wherein the second delay is a function of the second capacitance.

19. (Withdrawn) A built-in self-test (BIST) circuit embedded in an integrated circuit (IC) for determining whether a state change in a path input signal supplied to an input of a signal path within an integrated circuit (IC) produces a state change in a path output signal appearing at an output of the signal path with a delay exceeding a target delay indicated by input data, the BIST circuit comprising:

a BIST cell for producing a state change in the path input signal and for thereafter sampling the path output signal to determine its state, wherein the state change and the sampling are separated in

time by the target delay and are initiated by corresponding edges in first and second strobe signals also separated in time by the target delay;

a first multiplexer for receiving an input strobe signal and the first and second strobe signals, and for providing any one of the input, first and second strobe signals selected by first selection control data as a first multiplexer output signal;

a first circuit for generating the first and second strobe signals in response to the first multiplexer output signal such that each edge in the first multiplexer output signal subsequently produces a corresponding edge in the first and second strobe signals, with corresponding edges in the first and second strobe signals being separated in time by a programmable delay set by delay control data, and

a control circuit receiving the input data and the first multiplexer output signal, for supplying the input strobe signal and the first selection control data to the first multiplexer and for supplying the delay control data to the first circuit,

wherein the control circuit carries out a calibration process wherein it sets the delay control data so that the programmable delay between corresponding edges of the first and second control signals matches the target delay referenced by the input data, and

wherein following the calibration process, the control circuit sets the first selection control data so that the first multiplexer provides the input strobe signal as the first multiplexer output signal such that a next edge of the input strobe signal will result in corresponding edges in the first and second strobe signals separated in time by the target delay.

20. (Withdrawn) The BIST circuit in accordance with claim 19

wherein during the calibration process the control circuit iteratively generates count data, compares the count data to the input data, and adjusts the delay control data to determine a value for the delay control data that sets the programmable delay equal to the target delay,

wherein the count data indicates a difference between first and second quantities,

wherein the first quantity is a number of edges of a reference clock signal occurring during a first period determined by counting a predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer providing the first strobe signal as the first multiplexer output signal, and

wherein the second quantity is a number of edges of a reference clock signal occurring during a second period determined by counting the predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer providing the second strobe signal as the first multiplexer output signal.

21. (Withdrawn) The BIST circuit in accordance with claim 20 wherein the control circuit decrements the count data in response to edges of the reference clock signal during the first period and increments the count data in response to edges of the reference clock signal during the second period.

22. (Withdrawn) The BIST circuit in accordance with claim 20 wherein the control circuit comprises:

a first counter for counting edges of the first multiplexer output signal and for generating a gate signal indicating when the first and second periods are occurring;

a second counter for decrementing the count data in response to edges of the reference clock signal when the gate signal indicates the first period is occurring and for incrementing the count data in response to edges of the reference clock signal when he gate signal indicates the second period is occurring; and

means for incrementing or decrementing the delay control data depending on relative magnitudes of the count data and the delay data.

23. (Withdrawn) The BIST circuit in accordance with claim 20 wherein the first circuit comprises:

a tapped delay line having N taps for conveying the first multiplexer output signal to each of its N taps in succession, where N is greater than two;

a second multiplexer for providing the first multiplexer output signal conveyed to any one of the N taps selected by the delay control data as a second multiplexer output signal; and

first means for generating the first strobe signal in response to a the multiplexer output signal.

24. (Withdrawn) The BIST circuit in accordance with claim 23 wherein the first circuit further comprises:

second means for generating the second strobe signal in response to the first multiplexer output signal with a delay substantially matching a delay between an edge of the first multiplexer output signal arriving at any tap selected by the delay control data and a corresponding edge of the first strobe signal generated by the second means.

25. (Withdrawn) The BIST circuit in accordance with claim 23 wherein the first circuit further comprises:

a third multiplexer for providing the first multiplexer output signal conveyed to any one of the N taps selected by the delay control data as a third multiplexer output signal, wherein the delay control data independently controls the tap selection made by the second and third multiplexers; and

second means for generating the second strobe signal in response to the third multiplexer output signal.

26. (Currently Amended) An apparatus for responding to each edge of an input strobe signal by generating a corresponding edge in each of first and second strobe signals, wherein corresponding edges in the first and second strobe signals are separated by a target delay referenced by input data, the apparatus comprising:

means for generating an edge of the first strobe signal in delayed response to each edge of the input strobe signal;

a first multiplexer for receiving the input strobe signal and the second strobe signal and for providing either one of the input and second strobe signals selected by first selection control data as a first multiplexer output signal;

a tapped delay line comprising a plurality of gates connected in series for receiving the first multiplexer output signal and producing an edge in a separate tap signal at an output of each gate in delayed response to each edge in the first multiplexer output signal, wherein

a signal delay through each gate is a function of voltage supplied to the gates;

means for adjusting the voltage supplied to the gates in response to delay control data;

means for receiving the tap signal produced by each gate as input, for selecting one of the tap signals as a selected tap signal in response to the delay control data and for generating an edge in the second strobe signal in response to each edge in the selected tap signal; and

a control circuit receiving the input data and the first multiplexer output signal for supplying the first selection control data to the first mu..tiplexer and for supplying the delay control data to the ~~first circuit~~ means for adjusting the voltage supplied to the gates, wherein the first selection control data and the delay control data are functions of the input data.

27. (Original) The apparatus in accordance with claim 26 wherein the control circuit carries out a calibration process wherein it sets the delay control data so that a delay between corresponding edges of the first and second control signals matches the target delay referenced by the input data.

28. (Original) The apparatus in accordance with claim 27 wherein the calibration process comprises setting the first selection control data so that the first multiplexer selects the second strobe signal as the first multiplexer output signal and measuring a period of the first multiplexer output signal.